501.32049RV2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Yujiro KAJIHARA *et al.*

Serial No.: Unassigned (Rule 53b Divisional of 09/328,910)

Filed: 21 November 2001

For: LEAD FRAME SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE, USING THE SAME, AND METHOD OF AND PROCESS FOR FABRICATING THE TWO

Art Unit: Unassigned (Parent - 2815)

Examiner: Unassigned (Parent - J. Clark)

PRELIMINARY AMENDMENT

Honorable Commissioner for Patents
Washington, D.C. 20231

21 November 2001

Sir:

Prior to calculating the filing fee for the above-identified divisional reissue application, entry of the following amendments is respectfully requested.

IN THE SPECIFICATION:

Please replace the paragraph at Column 1, lines 5-7 with the following amended paragraph:

Notice: More than one reissue application has been filed for the reissue of U.S. Patent No. 5,637,913. The reissue applications are Serial No. 09/328,910 filed 9 June 1999, pending, and its divisional applications, Serial No. ____________ filed 16 November 2001, pending, and Serial No. ____________ filed 21 November 2001 (the present application), pending.

Please replace the paragraph at Page 3, Column 6, lines 31-41 with the following amended paragraph:

In case the aforementioned individual portions are formed by the pressing, burrs 11 are left on the back of the cut portions. Since the leadframe 1 of the present embodiment is made such that the die pad 3 has a smaller area than that of the semiconductor chip 2 to be mounted thereon, the burrs 11, if any, on the face of the die pad 3 for mounting the semiconductor chip 2 will be unable to mount the chip 2. When the die pad 3 is to be pressed, therefore, it is pressed with its chip mounting [Face] face being directed upward so that the burrs 11 may be left on the back opposed to the chip mounting face.

Please replace the paragraph at Page 4, Column 8, lines 46-50 with the following amended paragraph:

As shown in FIG. 15, moreover, slightly wider small pads (or adhesion-applied portions) 20 than the suspension leads 4 may be formed around he die pad 5 so that the adhesive [1S] 15 may be applied to the individual principal faces of the die pad 3 and the small pads 20.

IN THE CLAIMS:

Please amend Claims 1, 6, 11, 13 and 14 as follows.

1.(Once Amended) A semiconductor integrated circuit device comprising:

a semiconductor chip having a main surface including semiconductor elements and a plurality of bonding pads;

a leadframe having:

a chip mounting portion for mounting said semiconductor chip;

suspension leads unitarily formed with said chip mounting portion, a width of said chip mounting portion being wider than a width of each of said suspension leads[,]; and

a plurality of [inner lead portions] leads arranged to surround said semiconductor chip and being electrically connected with said bonding pads by bonding wires; and

[a plurality of outer lead portions individually connected with said inner lead portions; and]

a resin member sealing said semiconductor chip, at least a portion of said [inner lead portions] plurality of leads, said chip mounting portion, said suspension leads and said bonding wires[;],

wherein said chip mounting portion is smaller than said semiconductor chip and is positioned under a substantially central portion of said semiconductor chip, said semiconductor chip is fixed to said chip mounting portion by adhesive, said semiconductor chip is fixed to a part of each of said suspension leads by adhesive which is located under a peripheral portion of said semiconductor chip, and an adhesive region of said chip mounting portion and said semiconductor chip and an adhesive region of each of said suspension leads and said semiconductor chip are separated from each other, and wherein said suspension leads and said chip mounting portion of said leadframe are continuously formed in an area of said semiconductor chip.

6.(Once Amended) A semiconductor integrated circuit device according to [claim] Claim 5, wherein said resin member has a rectangular shape, and wherein said [outer lead portions are extended outwardly from] plurality of leads extend in a direction of four sides of said rectangular-shaped resin member.

11.(Once Amended) A semiconductor integrated circuit device comprising:

a semiconductor chip having a main surface including semiconductor elements and a plurality of bonding pads;

a leadframe having:

a cracking suppression means for mounting said semiconductor chip thereon and for suppressing, during a reflow soldering processing, device cracking, wherein said cracking suppression means is a chip mounting portion which is smaller than said semiconductor chip and which is positioned under a substantially central portion of said semiconductor chip[,];

suspension leads unitarily formed with said chip mounting portion, a width of said chip mounting portion being wider than a width of each of said suspension leads[,]; and

a plurality of [inner lead portions] leads arranged to surround said semiconductor chip and being electrically connected with said bonding pads by bonding wires; and

[a plurality of outer lead portions individually connected with said inner lead portions; and]

a resin member sealing said semiconductor chip, at least a portion of said [inner lead portions] plurality of leads, said chip mounting portion, said suspension leads and said bonding wires[;],

wherein said semiconductor chip is fixed to said chip mounting portion by adhesive, said semiconductor chip is fixed to a part of each of said suspension leads by adhesive which is located under a peripheral portion of said semiconductor chip, and an adhesive region of said chip mounting portion and said semiconductor chip and an adhesive region of each of said suspension leads and said semiconductor chip are separated from each other, and wherein said suspension leads and said chip mounting portion of said leadframe are continuously formed in an area of said semiconductor chip.

13.(Once Amended) A semiconductor integrated circuit device comprising:

a semiconductor chip having a main surface including semiconductor elements and a plurality of bonding pads;

a leadframe having:

a chip mounting portion for mounting said said semiconductor chip[,];

suspension leads unitarily formed with said chip mounting portion, a width of said chip mounting portion being wider than a width of each of said suspension leads[,]; and

a plurality of [inner lead portions] leads arranged to surround said semiconductor chip and being electrically connected with said bonding pads by bonding wires; and

[a plurality of outer lead portions individually connected with said inner lead portions; and]

a resin member sealing said semiconductor chip, at least a portion of said [inner lead portions] plurality of leads, said chip mounting portion, said suspension leads and said bonding wires[;].

wherein said chip mounting portion is smaller than said semiconductor chip and is positioned under a substantially central portion of said semiconductor chip, said semiconductor chip is fixed to said chip mounting portion by adhesive, said semiconductor chip is fixed to a part of each of said suspension leads by adhesive which is located under a peripheral portion of said semiconductor chip, and an adhesive region of said chip mounting portion and said semiconductor chip and an adhesive region of each of said suspension leads and said semiconductor chip are separated from each other.

14.(Once Amended) A semiconductor integrated circuit device comprising:

a semiconductor chip having a main surface including semiconductor elements and a plurality of bonding pads;

a leadframe having:

a cracking suppression means for mounting said semiconductor chip thereon and for suppressing, during a reflow soldering processing, device cracking, wherein said cracking suppression means is a chip mounting portion which is smaller than said semiconductor chip and which is positioned under a substantially central portion of said semiconductor chip,

suspension leads unitarily formed with said chip mounting portion, a width of said chip mounting portion being wider than a width of each of said suspension leads[,]; and

a plurality of [inner lead portions] leads arranged to surround said semiconductor chip and being electrically connected with said bonding pads by bonding wires; and

[a plurality of outer lead portions individually connected with said inner lead portions; and]

a resin member sealing said semiconductor chip, at least a portion of said [inner lead portions] plurality of leads, said chip mounting portion, said suspension leads and said bonding wires[;].

wherein said semiconductor chip is fixed to said chip mounting portion by adhesive, said semiconductor chip is fixed to a part of each of said suspension leads by adhesive which is located under a peripheral portion of said semiconductor chip, and an adhesive region of said chip mounting portion and said semiconductor chip and an adhesive region of each of said suspension leads and said semiconductor chip are separated from each other.

Please add new Claims 15-59, as follows.

15.(New) A method of manufacturing a semiconductor device comprising the steps of:

(a) preparing a lead frame having a first surface and a second surface opposite to said first surface, said lead frame having a chip mounting portion, suspension leads continuously formed with said chip mounting portion and a plurality

of leads, said first surface of said chip mounting portion being positioned to the side of said second surface of said plurality of leads rather than the side of said first surface of each of said plurality of leads;

(b) mounting a semiconductor chip on said chip mounting portion, said semiconductor chip having a plurality of semiconductor elements and bonding pads formed on a main surface thereof and a rear surface opposite to said main surface, and having a size which is larger than that of said chip mounting portion, said semiconductor chip being mounted so that said rear surface of said semiconductor chip is faced to said first surface of said chip mounting portion;

(c) electrically connecting said plurality of leads with said bonding pads of said semiconductor chip by a plurality of bonding wires respectively, in condition that said lead frame is placed on a heat stage having a groove for accommodating said chip mounting portion and said suspension leads and for a wire bonding operation, wherein said connecting step is performed in a condition that said chip mounting portion and said suspension leads are fitted in said groove, said rear surface of said semiconductor chip is in contact with an upper surface of said heat stage and said second surface of said chip mounting portion its spaced from a bottom surface of said groove; and

(d) sealing at least said semiconductor chip, said plurality of bonding wires and said chip mounting portion by a resin member.

16.(New) A method of manufacturing a semiconductor device according to Claim 15, wherein the step (a) includes bending said suspension leads, and wherein

a depth of said groove is deeper than a level of said bending of said suspension leads.

17.(New) A method of manufacturing a semiconductor device according to Claim 15, wherein the step (b) includes providing an adhesive to said first surface of said chip mounting portion, wherein said semiconductor chip and said chip mounting portion are bonded to each other by said adhesive.

18.(New) A method of manufacturing a semiconductor device according to Claim 17, wherein said adhesive is not provided to said suspension leads.

19.(New) A method of manufacturing a semiconductor device according to Claim 15, wherein said plurality of leads has a first lead adjacent to one of said suspension leads and a second lead which is relatively far from said one of said suspension leads in comparison with said first lead, and wherein a distance between the tip of said first lead and an edge of said semiconductor chip is shorter than a distance between the tip of said second lead and said edge of said semiconductor chip.

20.(New) A method of manufacturing a semiconductor device according to Claim 19, wherein a length of bonding wire connected to said first lead is shorter than a length of bonding wire connected to said second lead.

21.(New) A method of manufacturing a semiconductor device according to Claim 15, wherein a width of said chip mounting portion is larger than that of each of said suspension leads.

22.(New) A method of manufacturing a semiconductor device according to Claim 15, wherein in the step (c), parts of said plurality of leads, to which said plurality of bonding wires are bonded, are placed on said upper surface of said heat stage.

23.(New) A method of manufacturing a semiconductor device according to Claim 15, wherein said chip mounting portion has a substantially circular form in a plane view.

24.(New) A method of manufacturing a semiconductor device according to Claim 15, wherein said chip mounting portion has a substantially cross form in a plane view.

25.(New) A method of manufacturing a semiconductor device comprising the steps of :

(a) preparing a lead frame having a first surface and a second surface opposite to said first surface, said lead frame having a chip mounting portion, suspension leads continuously formed with said chip mounting portion and a plurality of leads;

(b) preparing a semiconductor chip selected from among a plurality of semiconductor chips having different sizes, said semiconductor chip having a plurality of semiconductor elements and bonding pads formed on a main surface thereof and a rear surface opposite to said main surface, and having a size which is larger than that of said chip mounting portion;

(c) mounting said semiconductor chip on said chip mounting portion, said semiconductor chip being mounted so that said rear surface of said semiconductor chip is faced to said first surface of said chip mounting portion;

(d) electrically connecting said plurality of leads with said bonding pads of said semiconductor chip by a plurality of bonding wires, in a condition that said lead frame is placed on a heat stage having a groove for accommodating said chip mounting portion and said suspension leads and for a wire bonding operation, wherein said connecting step is performed in condition that said chip mounting portion and said suspension leads are fitted in said groove, said rear surface of said semiconductor chip is contact with an upper surface of said heat stage and said second surface of said chip mounting portion is spaced from a bottom surface of said groove; and

(e) sealing at least said semiconductor chip, said plurality of bonding wires and said chip mounting portion by a resin member.

26.(New) A method of manufacturing a semiconductor device according to Claim 25, further comprising a step of bending said suspension leads such that said first surface of said chip mounting portion is located on a down side than said first surface of said inner lead portion of each of said plurality of leads in a thickness direction of said lead frame.

27.(New) A method of manufacturing a semiconductor device according to Claim 26, wherein said bending step includes providing a step portion to each of said suspension leads by said bending, and wherein a depth of said groove is deeper than a level of said bending of said suspension leads.

28.(New) A method of manufacturing a semiconductor device according to Claim 25, wherein the step (c) includes providing an adhesive to said first surface of said chip mounting portion, wherein said semiconductor chip and said chip mounting portion are bonded to each other by said adhesive.

29.(New) A method of manufacturing a semiconductor device according to Claim 28, wherein said adhesive is not provided to said suspension leads.

30.(New) A method of manufacturing a semiconductor device according to Claim 25, wherein said plurality of leads has a first lead adjacent to one of said suspension leads and a second lead which is-relatively far from said one of said suspension leads in comparison with said first lead, and wherein a distance between the tip of said first lead and an edge of said semiconductor chip is shorter than a distance between the tip of said second lead and said edge of said semiconductor chip.

31.(New) A method of manufacturing a semiconductor device according to Claim 30, wherein a length of bonding wire connected to said first lead is shorter than a length of bonding wire connected to said second lead.

32.(New) A method of manufacturing a semiconductor device according to Claim 25, wherein a width of said chip mounting portion is larger than that of each of said suspension leads.

33.(New) A method of manufacturing a semiconductor device according to Claim 25, wherein in the step (e), parts of said plurality of leads, to which said plurality of bonding wires are bonded, are placed on said upper surface of said heat stage.

34.(New) A method of manufacturing a semiconductor device according to Claim 25, wherein said chip mounting portion has a substantially circular form in a plane view.

35.(New) A method of manufacturing a semiconductor device according to Claim 25, wherein said chip mounting portion has a substantially cross form in a plane view.

36.(New) A method of manufacturing a semiconductor device comprising the steps of;

(a) preparing a lead frame having a first surface and a second surface opposite to said first surface, said lead frame having a chip mounting portion, suspension leads continuously formed with said chip mounting portion and a plurality of leads, said first surface of said chip mounting portion being positioned to the side

of said second surface of said plurality of leads rather than the side of said first surface of said plurality of leads;

(b) mounting a semiconductor chip on said chip mounting portion, said semiconductor chip having a plurality of semiconductor elements and bonding pads formed on a main surface thereof and a rear surface opposite to said main surface, and having a size which is larger than that of said chip mounting portion, said semiconductor chip being mounted so that said rear surface of said semiconductor chip is faced to said first surface of said chip mounting portion;

(c) electrically connecting said plurality of leads with said bonding pads of said semiconductor chip by a plurality of bonding wires respectively, in condition that said lead frame is placed on a heat stage having a groove for accommodating said chip mounting portion and said suspension leads and for a wire bonding operation, wherein said connecting step is performed in a condition that said chip mounting portion and said suspension leads are fitted in said groove, said rear surface of said semiconductor chip is in contact with an upper surface of said heat stage and said second surface of said chip mounting portion and said suspension leads are spaced from a bottom surface of said groove; and

(d) sealing at least said semiconductor chip, said plurality of bonding wires and said chip mounting portion by a resin member.

37.(New) A semiconductor device comprising:

(a) a semiconductor chip having a plurality of semiconductor elements and bonding pads formed on a main surface thereof;

(b) a lead frame having:

a chip mounting portion for mounting said semiconductor chip;

a plurality of leads; and

suspension leads continuously formed with said chip mounting portion, said semiconductor chip being mounted on said chip mounting portion;

(c) an insulating tape adhered to at least said plurality of leads and said suspension leads;

(d) bonding wires electrically connected to said plurality of leads with said bonding pads of said semiconductor chip respectively, and

(e) a resin member sealing said semiconductor chip, said bonding wires, said insulating tape, said chip mounting portion, a part of each of said suspension leads, and at least a portion of said plurality of leads,

wherein a size of said chip mounting portion is smaller than that of said semiconductor chip, and

wherein said insulating tape continuously extends from said plurality of leads to said suspension leads.

38.(New) A semiconductor device according to Claim 37, wherein said resin member has a rectangular shape, wherein said suspension leads extend from said chip mounting portion toward four corners of said resin member, and wherein said plurality of leads are arranged between said suspension leads in a plane view.

39.(New) A semiconductor device according to Claim 37, wherein said insulating tape extends along four sides of said resin member to surround said chip mounting portion and said semiconductor chip in a plane view.

40.(New) A semiconductor device according to Claim 37, wherein said insulating tape includes a base insulating film and an adhesive layer applied to one surface of said base insulating film, and wherein said insulating tape is adhered to said plurality of leads and said suspension leads by said adhesive layer.

41.(New) A semiconductor device according to Claim 40, wherein said base insulating film includes a polyimide resin and said adhesive layer includes an acrylic resin.

42.(New) A semiconductor device according to Claim 37, wherein said lead frame having a first surface and a second surface opposite to said first surface, wherein each of said suspension leads has a step portion so that said first surface of said chip mounting portion is positioned to the side of said second surface of said plurality of leads rather than the side of said first surface of said plurality of leads, and wherein said insulating tape is arranged outside said step portion of each of said suspension leads.

43.(New) A semiconductor device according to Claim 42, wherein a part of each of said suspension leads, which is located outside said step portion, is substantially at a same level as portions of said plurality of leads in a thickness direction of said lead frame.

44.(New) A semiconductor device comprising:

(a) a semiconductor chip having a plurality of semiconductor elements and

bonding pads formed on a main surface thereof and a rear surface opposite to said main surface;

(b) a lead frame having a first surface and a second surface opposite to said first surface, said lead frame having:

a chip mounting portion for mounting said semiconductor chip;

suspension leads continuously formed with said chip mounting portion; and

a plurality of leads;

(c) a plurality of bonding wires electrically connected to said plurality of leads with said bonding pads of said semiconductor chip respectively; and

(d) a resin member sealing at least said semiconductor chip, said bonding wires, said chip mounting portion and at least portions of said plurality of leads,

wherein a size of said chip mounting portion is smaller than that of said semiconductor chip, and

wherein said semiconductor chip is mounted on said chip mounting portion, such that said rear surface of said semiconductor chip is bonded to the side of said first surface of said chip mounting portion by an adhesive layer, and such that a part of each of said suspension leads, which is located under said semiconductor chip, is spaced from said rear surface of said semiconductor chip.

45.(New) A semiconductor device according to Claim 44, wherein said adhesive layer is provided on said first surface of said chip mounting portion and is not provided on said part of each of said suspension leads which is located under said semiconductor chip.

46.(New) A semiconductor device according to Claim 45, wherein a part of said rear surface of said semiconductor chip, which is located outside said chip mounting portion, is adhered to a part of said resin member.

47.(New) A semiconductor device according to Claim 46, wherein said resin member includes a thermosetting resin.

48.(New) A semiconductor device according to Claim 44, wherein said adhesive layer includes an epoxy resin.

49.(New) A semiconductor device comprising:

(a) a semiconductor chip having a plurality of semiconductor elements and bonding pads formed on a main surface thereof and a rear surface opposite to said main surface;

(b) a lead frame having a first surface and a second surface opposite to said first surface, said lead frame having:

a chip mounting portion for mounting said semiconductor chip;

suspension leads continuously formed with said chip mounting portion; and

a plurality of leads;

(c) a plurality of bonding wires electrically connected to said plurality of leads with said bonding pads of said semiconductor chip respectively; and

(d) a resin member sealing at least said semiconductor chip, said bonding wires, said chip mounting portion and at least portions of said plurality of leads,

wherein a size of said chip mounting portion is smaller than that of said semiconductor chip,

wherein said semiconductor chip is bonded to said chip mounting portion by an adhesive layer between said rear surface of said semiconductor chip and said first surface of said chip mounting portion,

wherein each of said suspension leads has a part which is located under said semiconductor chip, and

wherein a part of said resin member is formed between said part of each of said suspension leads and said rear surface of said semiconductor chip.

50.(New) A semiconductor device comprising:

(1) a semiconductor chip having a main surface and a rear surface opposite to said main surface, said semiconductor chip having a plurality of semiconductor elements and bonding pads formed on said main surface;

(2) a lead frame including:

a first suspension lead for supporting said semiconductor chip, extending in a first direction;

a second suspension lead for supporting said semiconductor chip, extending in a second direction which is different from said first direction, said second suspension lead intersecting said first suspension lead; and

a plurality of leads, said plurality of leads being arranged to surround an intersecting portion of said first and second suspension leads;

(3) a plurality of bonding wires electrically connecting at said plurality of leads with said plurality of bonding pads, respectively; and

(4) a resin body sealing said semiconductor chip, at least a portion of said plurality of leads, said first and second suspension leads and said plurality of bonding wires,

wherein said semiconductor chip is disposed on said intersecting portion of said first and second suspension leads,

wherein a width of each of said first and second suspension leads at the vicinity of said intersecting portion is wider than that of each said first and second suspension leads at vicinities beyond said semiconductor chip, and

wherein said rear surface of said semiconductor chip is fixed to said first and second suspension leads at the vicinity of said intersecting point by an adhesive.

51.(New) A semiconductor device according to Claim 50, wherein said first and second suspension leads intersect each other at a substantially right angle.

52.(New) A semiconductor device according to Claim 51, wherein said resin body has a tetragonal shape, wherein said plurality of leads extends toward four sides of said resin body, and wherein said first and second suspension leads extend from said intersecting portion toward four corners of said resin body.

53.(New) A semiconductor device according to Claim 50, wherein a portion of said rear surface of said semiconductor chip is adhered to said intersecting portion of said first and second suspension leads, and wherein another portion of said rear surface of said semiconductor chip is contacted with said resin body.

54.(New) A semiconductor device according to Claim 51, wherein said semiconductor chip has a tetragonal shape, and wherein said wider portion at the vicinity of said intersecting portion of said first and second suspension leads extends from a central portion of said rear surface of said semiconductor chip toward four corners of said semiconductor chip.

55.(New) A semiconductor device comprising:

(1) a semiconductor chip having a main surface and a rear surface opposite to said main surface, said semiconductor chip having a plurality of semiconductor elements and bonding pads formed on said main surface;

(2) a lead frame including:

a chip mounting portion for mounting said semiconductor chip;

a plurality of suspension leads which are continuously formed with said chip mounting portion; and

a plurality of leads, said plurality of leads being arranged to surround said chip mounting portion;

(3) a plurality of bonding wires electrically connecting said plurality of leads with said plurality of bonding pads, respectively; and

(4) a resin body sealing said semiconductor chip, at least a portion of said plurality of leads, said chip mounting portion, said plurality of suspension leads and said plurality of bonding wires,

wherein said chip mounting portion has a first portion extending in a first direction and a second portion extending in a second direction which is a different direction from said first direction, said second portion intersecting said first portion,

wherein a width of each of said first and second portions of said chip mounting portion is wider than that of each of said plurality of suspension leads,

wherein both ends of each of said first and second portions of said chip mounting portion are coupled with said plurality of suspension leads respectively,

wherein an intersecting portion of said first and second portions of said chip mounting portion is located at a substantially central portion of said rear surface of said semiconductor chip,

wherein said both ends of each of said first and second portions of said chip mounting portion are located at the peripheral portions of said rear surface of said semiconductor chip, and

wherein said rear surface of said semiconductor chip is fixed to said chip mounting portion at both of said central and peripheral portions of said rear surface of said semiconductor chip by an adhesive.

56.(New) A semiconductor device according to Claim 55, wherein said first and second directions intersect each other at a substantially right angle.

57.(New) A semiconductor device according to Claim 56, wherein said resin body has a tetragonal shape, wherein said plurality of leads extends toward four sides of said resin body, and wherein said plurality of suspension leads extend from said both ends of said first and second portions of said chip mounting portion toward four corners of said resin body.

58.(New) A semiconductor device according to Claim 55, wherein a portion of said rear surface of said semiconductor chip is adhered to said first and second portions of said chip mounting portion, and wherein another portion of said rear surface of said semiconductor chip is contacted with said resin body.

59.(New) A semiconductor device according to Claim 58, wherein said semiconductor chip has a tetragonal shape, and wherein said both ends of each of said first and second portions are located at the vicinity of four corners of said semiconductor chip.

REMARKS

This Preliminary Amendment submits the following amendments and remarks for entry and consideration in the present divisional reissue application.

STATUS OF CLAIMS AND SUPPORT FOR CLAIM CHANGES

Claims 1-14 were issued in the original patent upon which the parent reissue application of the present divisional reissue case is based. Unrelated to any prior art rejection, appropriate Claims have been amended and/or added herein to adjust a clarity and/or focus of Applicant's claimed invention. New Claims 15-59 submitted herein, which parallel reissue parent Claims 15-36 and 50-72, respectively, and have been slightly broadened/simplified by removing limitations believed unnecessary for patentability. More particularly, prior claim limitations concerning, for example, "a plurality of leads each having an inner lead portion and an outer lead portion" have

been broadened/simplified to simply "a plurality of leads." Further, prior claim limitations of "a resin member sealing...said inner lead portions" have been broadened/simplified to "a resin member sealing...at least a portion of said leads."

All amendments to Claims 1-14, and all new Claims 15-59, find full support in the patent as issued and the parent reissue application. No new matter is added.

At entry of this paper, Claims 1-59 are pending in this divisional reissue application for consideration and examination.

REQUEST FOR EXAMINER INTERVIEW PRIOR TO FIRST ACTION AND NOTIFICATION OF INTENT TO FILE PRELIMINARY AMENDMENT

An Examiner Interview prior to first Office Action in this continuing or substitute application is respectfully requested. As stated in MPEP §713.02, "A request for an interview prior to first Office Action is ordinarily granted in continuing or substitute applications." Similarly, as stated in MPEP §706.07(b), "A request for an interview prior to first action on a continuing or substitute application should ordinarily be granted." After such Examiner Interview, Applicant may file a further Preliminary Amendment for adjusting/submitting claims which should be examined in the present divisional reissue application. The Examiner is respectfully requested to contact the attorney indicated on this paper at the local Washington, D.C. area telephone number of 703-312-6600 for the purpose of scheduling an Examiner Interview. The Examiner is thanked in advance for such considerations. Contact will also be attempted by the undersigned attorneys to schedule an Examiner Interview.

DISCLOSURE/SPECIFICATION AMENDMENTS

In the parent reissue application of the present divisional reissue case, the disclosure/specification was objected because of minor informalities. Therefore, the amendments to the specification that have been adopted in the parent reissue application are repeated in the present divisional reissue case.

Further, the specification has been amended to supply a required Notice Section indicating that more than one application has been filed for reissue of a single patent, and such Notice will be updated upon receipt of the required information by Applicant.

Any spelling, idiomatic, grammatical and/or other informality noted during any further review of the disclosure/specification will be appropriately corrected.

CLAIM FOR PRIORITY

Applicant hereby claims priority under 35 USC §119 of JP 4-320098 filed 30 November 1992 and JP 4-71116 filed 27 March 1992. The certified copies of the priority documents were submitted on 29 March 1993 in prior application Serial No. 08/038,684, which matured into U.S. Patent No. 5,637,913, the patent on which the parent reissue and the present divisional reissue cases are based. Acknowledgment of the claim for priority in this divisional reissue application is courteously solicited.

INFORMATION DISCLOSURE STATEMENT

Attached hereto are Forms PTO-1449 listing all of the references cited to or by the Office in the patented file and the parent reissue application upon which this divisional reissue application is based. In accordance with 37 CFR §§ 1.97 and 1.98,

Applicant respectfully requests return of copies of the Forms PTO-1449 bearing the Examiner's initials indicating entry and consideration of the information listed on the attached Forms PTO-1449, so that the information appears on the printed face of any reissue patent issuing on the present divisional reissue application.

In addition, attention is directed to MPEP §904, which states that, "In all continuing applications, the parent applications should be reviewed by the Examiner for pertinent prior art.", and further states that the fact of review "...should be made of record in accordance with the procedure set forth...[in]...MPEP §717.05." Any independent review by the Examiner of the prior application(s) and utilization of any necessary Form PTO-892s to ensure that all known prior application art is considered and listed on any patent issuing from the present application would be greatly appreciated by the Applicant and the undersigned.

EXAMINER INVITED TO TELEPHONE

The Examiner is herein invited to telephone the undersigned attorneys at the local Washington, D.C. area telephone number of 703-312-6600 for discussing any Examiner's Amendments or other suggested actions for accelerating prosecution and moving the present application to allowance.

CONCLUSION

In view of the foregoing amendments and remarks, Applicant respectfully submits that the claims listed above as presently being under consideration in this divisional reissue application are now in condition for allowance. Accordingly, early allowance of such claims is respectfully requested.

Please charge any shortage in fees necessitated by this Preliminary Amendment or divisional reissue application, including excess claim fees, to ATS&K Deposit Account No. 01-2135 (as Order No. 501.32049RV2), and credit any overpayment or excess fee thereto.

Respectfully submitted,

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ATTACHMENTS:
APPENDIX A-MARKED VERSION
Forms PTO-2038 (2)

APPENDIX A-MARKED VERSION

Paragraph at page 6, lines 31-41:

In case the aforementioned individual portions are formed by the pressing, burrs 11 are left on the back of the cut portions. Since the leadframe 1 of the present embodiment is made such that the die pad 3 has a smaller area than that of the semiconductor chip 2 to be mounted thereon, the burrs 11, if any, on the face of the die pad 3 for mounting the semiconductor chip 2 will be unable to mount the chip 2. When the die pad 3 is to be pressed, therefore, it is pressed with its chip mounting [Face] face being directed upward so that the burrs 11 may be left on the back opposed to the chip mounting face.

Paragraph at page 8, lines 46-50:

As shown in FIG. 15, moreover, slightly wider small pads (or adhesion-applied portions) 20 than the suspension leads 4 may be formed around he die pad 5 so that the adhesive [1S] 15 may be applied to the individual principal faces of the die pad 3 and the small pads 20.

IN THE CLAIMS:

1.(Once Amended) A semiconductor integrated circuit device comprising:

a semiconductor chip having a main surface including semiconductor elements and a plurality of bonding pads;

a leadframe having:

a chip mounting portion for mounting said semiconductor chip;

suspension leads unitarily formed with said chip mounting portion, a

width of said chip mounting portion being wider than a width of each of said suspension leads[,]; and

a plurality of [inner lead portions] leads arranged to surround said semiconductor chip and being electrically connected with said bonding pads by bonding wires; and

[a plurality of outer lead portions individually connected with said inner lead portions; and]

a resin member sealing said semiconductor chip, at least a portion of said [inner lead portions] plurality of leads, said chip mounting portion, said suspension leads and said bonding wires[;],

wherein said chip mounting portion is smaller than said semiconductor chip and is positioned under a substantially central portion of said semiconductor chip, said semiconductor chip is fixed to said chip mounting portion by adhesive, said semiconductor chip is fixed to a part of each of said suspension leads by adhesive which is located under a peripheral portion of said semiconductor chip, and an adhesive region of said chip mounting portion and said semiconductor chip and an adhesive region of each of said suspension leads and said semiconductor chip are separated from each other, and wherein said suspension leads and said chip mounting portion of said leadframe are continuously formed in an area of said semiconductor chip.

6.(Once Amended) A semiconductor integrated circuit device according to [claim] Claim 5, wherein said resin member has a rectangular shape, and wherein

said [outer lead portions are extended outwardly from] plurality of leads extend in a direction of four sides of said rectangular-shaped resin member.

11.(Once Amended) A semiconductor integrated circuit device comprising:

a semiconductor chip having a main surface including semiconductor elements and a plurality of bonding pads;

a leadframe having:

a cracking suppression means for mounting said semiconductor chip thereon and for suppressing, during a reflow soldering processing, device cracking, wherein said cracking suppression means is a chip mounting portion which is smaller than said semiconductor chip and which is positioned under a substantially central portion of said semiconductor chip[,];

suspension leads unitarily formed with said chip mounting portion, a width of said chip mounting portion being wider than a width of each of said suspension leads[,]; and

a plurality of [inner lead portions] leads arranged to surround said semiconductor chip and being electrically connected with said bonding pads by bonding wires; and

[a plurality of outer lead portions individually connected with said inner lead portions; and]

a resin member sealing said semiconductor chip, at least a portion of said [inner lead portions] plurality of leads, said chip mounting portion, said suspension leads and said bonding wires[;].

wherein said semiconductor chip is fixed to said chip mounting portion by adhesive, said semiconductor chip is fixed to a part of each of said suspension leads by adhesive which is located under a peripheral portion of said semiconductor chip, and an adhesive region of said chip mounting portion and said semiconductor chip and an adhesive region of each of said suspension leads and said semiconductor chip are separated from each other, and wherein said suspension leads and said chip mounting portion of said leadframe are continuously formed in an area of said semiconductor chip.

13.(Once Amended) A semiconductor integrated circuit device comprising:

a semiconductor chip having a main surface including semiconductor elements and a plurality of bonding pads;

a leadframe having:

a chip mounting portion for mounting said said semiconductor chip[,];

suspension leads unitarily formed with said chip mounting portion, a width of said chip mounting portion being wider than a width of each of said suspension leads[,]; and

a plurality of [inner lead portions] leads arranged to surround said semiconductor chip and being electrically connected with said bonding pads by bonding wires; and

[a plurality of outer lead portions individually connected with said inner lead portions; and]

a resin member sealing said semiconductor chip, at least a portion of said [inner lead portions] plurality of leads, said chip mounting portion, said suspension leads and said bonding wires[;],

wherein said chip mounting portion is smaller than said semiconductor chip and is positioned under a substantially central portion of said semiconductor chip, said semiconductor chip is fixed to said chip mounting portion by adhesive, said semiconductor chip is fixed to a part of each of said suspension leads by adhesive which is located under a peripheral portion of said semiconductor chip, and an adhesive region of said chip mounting portion and said semiconductor chip and an adhesive region of each of said suspension leads and said semiconductor chip are separated from each other.

14.(Once Amended) A semiconductor integrated circuit device comprising:

a semiconductor chip having a main surface including semiconductor elements and a plurality of bonding pads;

a leadframe having:

a cracking suppression means for mounting said semiconductor chip thereon and for suppressing, during a reflow soldering processing, device cracking, wherein said cracking suppression means is a chip mounting portion which is smaller than said semiconductor chip and which is positioned under a substantially central portion of said semiconductor chip,

suspension leads unitarily formed with said chip mounting portion, a width of said chip mounting portion being wider than a width of each of said suspension leads[,]; and

a plurality of [inner lead portions] leads arranged to surround said semiconductor chip and being electrically connected with said bonding pads by bonding wires; and

[a plurality of outer lead portions individually connected with said inner lead portions; and]

a resin member sealing said semiconductor chip, at least a portion of said [inner lead portions] plurality of leads, said chip mounting portion, said suspension leads and said bonding wires[;],

wherein said semiconductor chip is fixed to said chip mounting portion by adhesive, said semiconductor chip is fixed to a part of each of said suspension leads by adhesive which is located under a peripheral portion of said semiconductor chip, and an adhesive region of said chip mounting portion and said semiconductor chip and an adhesive region of each of said suspension leads and said semiconductor chip are separated from each other.